

AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

1. (CURRENTLY AMENDED) A circuit comprising:

a database configured to store a pointer for each of a plurality of first parameters ~~parameter~~ of a network protocol; and

5 a processing circuit configured to (i) process at least one of said first parameters in an incoming packet in accordance with said pointer to produce a second parameter and (ii) present an outgoing packet containing said second parameter.

2. (CURRENTLY AMENDED) The circuit according to claim

1, wherein said database is further configured to store both an offset and a length for each of the said first parameters ~~parameter~~, and said processing circuit is further configured to

5 partition said incoming packet in accordance with both of said offsets and said lengths to extract said first parameters.

3. (CURRENTLY AMENDED) The circuit according to claim

2, further comprising an interface directly connected to said database and configured to download all of said offsets, said lengths, and said pointers for storage in said database.

4. (CURRENTLY AMENDED) The circuit according to claim 1, wherein said processing circuit comprises:

a parsing circuit configured to partition said incoming packet;

5 a plurality of peripheral blocks each (i) coupled to said parsing circuit, (ii) linked to said pointers and ~~(ii)~~ (iii) configured to perform a process involving said first parameters; and

10 an assembling circuit coupled to said peripheral blocks and configured to generate said outgoing packet.

5. (CURRENTLY AMENDED) The circuit according to claim 4, wherein said database is further configured to store both a second offset, and a second length for said second parameter of a second network protocol.

6. (ORIGINAL) The circuit according to claim 4, further comprising an interface connectable to a peripheral block external to said circuit.

7. (ORIGINAL) The circuit according to claim 4, wherein said peripheral blocks are at least two circuits of a content addressable memory circuit, a time to live circuit, a comparison circuit, a counter circuit, a value swapping circuit, a stuffing

5 circuit, a de-stuffing circuit, a cyclic redundancy checksum
circuit, a parity circuit, a first-in-first-out circuit, a length
construction generator circuit, a header error control
synchronization circuit, a frame relay lookup circuit, a data link
connection identifier circuit, a protocol identification analysis
10 circuit, a point-to-point protocol verification circuit, a
parameter discard circuit, and a buffer circuit.

8. (CURRENTLY AMENDED) The circuit according to claim
6, wherein said peripheral blocks are ~~block is~~ configured to
simultaneously processes a plurality of said first parameters.

9. (CURRENTLY AMENDED) The circuit according to claim
1, wherein said processing circuit is ~~configured~~ implemented as
only hardware.

10. (CURRENTLY AMENDED) An assembly comprising:

a first circuit configured to delineate a receive frame
from a first network having a network protocol to produce an
incoming packet;

5 a second circuit configured to (i) store a pointer for
each of a plurality of first parameters ~~parameter~~ of said network
protocol, (ii) process at least one of said first parameters in
said incoming packet in accordance with said pointer to produce a

second parameter, and (iii) present an outgoing packet containing
10 said second parameter; and

a third circuit configured to frame said outgoing packet
to present a transmit frame to a second network.

11. (CURRENTLY AMENDED) The assembly according to claim
10, wherein said second circuit is further configured to (i) store
both an offset and a length for each of said first parameters and
(ii) partition said incoming packet in accordance with both of said
5 offsets and said lengths to extract said first parameters from said
incoming packet.

12. (ORIGINAL) The assembly according to claim 10,
wherein said first circuit is further configured to provided a
plurality of frame delineation methods for a plurality of network
protocols.

13. (ORIGINAL) The assembly according to claim 12,
further comprising an interface configured to permit a selection
among said frame delineation methods.

14. (ORIGINAL) The assembly according to claim 10,
wherein said second circuit is further configured to provided a
plurality of framing methods for a plurality of network protocols.

15. (ORIGINAL) The assembly according to claim 14, further comprising an interface configured to permit a selection among said framing methods.

16. (ORIGINAL) The assembly according to claim 10, wherein said third circuit is further configured to delineate a second receive frame from said second network to produce said incoming packet.

17. (ORIGINAL) The assembly according to claim 16, wherein said first circuit is further configured to frame said outgoing packet to present a second transmit frame to said first network.

18. (CURRENTLY AMENDED) The assembly according to claim 10, wherein said first circuit comprises a plurality of framing circuits each configured to operate on a unique network protocol.

19. (CURRENTLY AMENDED) The assembly according to claim 10, wherein said third circuit comprises a plurality of de-framing circuits each configured to operate on a unique network protocol.

20. (PREVIOUSLY PRESENTED) The assembly according to claim 10, further comprising a fourth circuit connected to said second circuit and configured process at least one of said first parameters in said incoming packet in accordance with said pointer.